07-28-00 AB

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael R. May

Docket No. SIG000049

Title: EDGE SENSITIVE DETECTION CIRCUIT

Date: 7/25/2000

To the Honorable Commissioner
of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

REQUEST FOR FILING A NATIONAL PATENT APPLICATION

The applicant respectfully requests that the above captioned patent application be accepted for examination. This patent application is a:

- [X] new patent application
- [ ] continuation in part (CIP) of Application Serial No. [ ] filed on [ ]
- [ ] divisional application of Application Serial No. [ ] filed on [ ]
- [ ] continuation application of Application Serial No. [ ] filed on [ ]

Accompanying this request is (as indicated by an "X" in the corresponding box):

- [X] 1. 13 pages of specification, which includes the claims and abstract, and 2 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [X] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;
- [X] 8. A certificate of mailing indicating that the above captioned patent application has been deposited as "Express Mail" with the United States Postal Service;
- [ ] 9. A certificate of mailing indicating that the above captioned patent application has been deposited with the United States Postal Service with sufficient postage as first class mail;
- [X] 10. A return postcard; and
- [ ] 11. A preliminary amendment.

The filing fee for the above captioned patent application is as follows:

Large entity status apply? no

				basic filing fee	345.00
total claims	18	extra per claim fee	9.00	extra claim fee	0.00
total ind claims	3	extra per ind claim fee	39.00	extra ind claim fee	0.00
				assign record fee	40.00
				TOTAL FILING FEE	385.00

Payment of the above calculated filing fee is as follows (as indicated by the "X" in the corresponding box):

[X] A check in the amount of $ 385.00

[ ] Please charge Deposit Account No. in the amount of $

A duplicate sheet is attached.

Respectfully submitted,

By: _____

Timothy W. Markison
Registration No: 33,534
Phone: (512) 381-3732
Fax: (512) 381-4125

SIG000049

Customer No: 000024263
SigmaTel, Inc.,
2700 Via Fortuna, Suite 500
Austin, Texas 78746

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael R. May	Examiner:	
Serial No.		Art Group:	
Filing Date:		Docket No.	SIG000049

Title: EDGE SENSITIVE DETECTION CIRCUIT

7/25/2000

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

STATEMENT OF STATUS AS SMALL ENTITY
Pursuant to 37 C.F.R. Section 1.27 and Section 1.9

For the above captioned patent application, a party in interest avers that it qualifies for small entity status as SMALL BUSINESS CONCERN. To verify the small entity status, the party in interest attests that:

1. This verified statement for the above captioned patent application or patent is being submitted prior to or with the first fee paid as a small entity;

2. For purposes of this verified statement, as defined in 37 C.F.R. Section 1.27, a license to a Federal agency resulting from a funding agreement with that agency pursuant to 35 U.S.C. 202 (c) (4) does not constitute a license.

3. As a SMALL BUSINESS CONCERN:
(a) I swear that I am an official of SigmaTel, Inc., empowered to act on behalf of SigmaTel, Inc.,
(b) In my capacity as identified in this section 3(a), I swear that SigmaTel, Inc. qualifies as a small business concern as defined in 37 C.F.R Section 1.9 and that the number of employees of SigmaTel, Inc. and those of its affiliates, does not exceed 500 persons;
(c) I further swear that my signature appears at the end of this Statement of Status as Small Entity;
(d) I still further swear that, in support my of contention that SigmaTel, Inc. qualifies as a small business concern, exclusive rights to the invention of the above captioned patent application have been conveyed to and remain with SigmaTel, Inc.,

Signatures of Person(s) Making the Verified Statement

SigmaTel, Inc. (Customer No:000024263)
Name: Timothy W. Markison

TW Mk
Signature

7/27/00
Date

Title: General Counsel

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael R. May

Examiner:

Serial No.

Art Group:

Filing Date:

Docket No. SIG000049

Title: EDGE SENSITIVE DETECTION CIRCUIT

7/21/2000

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING

Express Mail Labe EL581298002US Name of Depositor: Diane Hudson

Date of Deposit: 7/27/00 Signature: Diane Hudson

I hereby certify that this paper and the items identified below are being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Items accompanying this Certificate of Express Mailing:

- [X] 1. A new patent application including 13 pages of specification, and 2 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [X] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;
- [X] 8. A return postcard; and
- [ ] 9. A preliminary amendment.

SigmaTel, Inc.
Customer No: 000024263

EDGE SENSITIVE DETECTION CIRCUIT

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to detection circuits and more particularly to an edge sensitive detection circuit.

BACKGROUND OF THE INVENTION

Detection circuits are widely used in electronic equipment to detect an event that triggers initiation of a corresponding response. For example, detection circuits are widely used in computers, automobile engine control systems, microwave ovens, coffee makers, etc. In computers, an event may be power on, power down, standby, reset, an interrupt, change in settings, etc., where each of the events has a corresponding response. For example, the power on event has a corresponding response that turns the computer on in a predetermined manner.

As is known, a computer includes multiple layers of software and/or hardware that include detection circuitry/software and/or response circuitry/software. To process a corresponding response from a detected event, different elements of the software and/or hardware process different aspects of the corresponding response and detecting the event. For example, for a power on sequence, a detection circuit must first detect the power on condition. For the "power on" detection circuit to detect a power on event, it must be receiving power. As such, the "power on" detection circuit is either operably coupled to a battery source or is included in the power supply. Before any of the associated software can be processed, the central processing unit (CPU) must be receiving power, the clocks must be up and running, and the interoperability between the CPU and memory must be up and running.

With power applied to the hardware components of the computer, the power on software may now be processed. Such power on software includes system BIOS, enabling the operating system, enabling video graphics processing, and enabling other peripheral components. Because of the distributed nature of the computer system, events are typically triggers as a logic setting. For example, a reset condition may occur when a reset pin is pulled to a logic "0" state and the reset condition is removed when the reset pin is pulled to a logic "1" state. Thus, an event is triggered when the detection circuit detects a predetermined logic state on a corresponding pin and no event occurs, or the event is removed, when the detection circuit detects an alternate predetermined logic state.

While logic state triggering of events works well in distributed systems, such as a computer, it does not work well in integrated systems. An integrated system has a difficult time processing events, such as power down, reset, standby, set, and power up when the event is triggered via a logic state change. The difficulty arises because the software that overwrites the logic state of the event needs to be active, such that the detection circuit may detect a change in the logic state of the event. However, the processor and memory interfaces cannot be activated to process the software to change the logic state of the event until the detection circuit detects a change in the logic state. Thus, a chicken and egg dilemma arises.

Therefore, a need exists for a detection circuit that overcomes the above described problems.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic block diagram of an edge detection circuit in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of an alternate edge detection circuit in accordance with the present invention; and

Figure 3 illustrates a schematic block diagram of another edge detection circuit in accordance with the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Generally, the prevent invention provides an edge sensitive detection circuit that includes a filter module and a soft latch module. The filter module is operably coupled to receive an input logic signal that corresponds to the triggering of an event and produces a pulse signal in response to an edge of the input logic signal. The filter may include a capacitor operably coupled to a controlled impedance, an inverter and a driver transistor, wherein the capacitor senses an edge of the input logic signal and, in combination with the controlled impedance, produces the pulse signal. The soft latch module is operably coupled to receive the pulse signal and to latch a logic value in accordance with the pulse signal. With use of such an edge detection circuit in an integrated system, the integrated system overcomes the chicken and the egg dilemma of previous event detection circuits. For example, if an edge detection circuit were used as part of a power down control circuit, the software can power down the system by a state change and power up the system effectively at a later time.

The present invention may be more fully described with reference to figures 1 - 3. Figure 1 illustrates a schematic block diagram of an edge detection circuit 10 that includes a filter module 12 and a soft latch module 14. The filter module 12 is operably coupled to receive an input logic signal 16 that is representative of an event, where the signal 16 may be one of a reset signal, a power down signal, a power up signal, a standby signal, and a set signal. The filter module 12 is tuned to sense an edge of the input logic signal 16 such that it produces a pulse signal 18.

The soft latch module 14 receives the pulse signal 18 and produces a latched logic value 20. Depending on the state of the soft latch module 14 when the pulse signal is received, the state of the latched logic value 20 may toggle. For example, if the latched logic output value 20 were in a logic "0" state when the pulse signal 18 was received, the latched logic value 20 would toggle to a logic "1" state. If, however, the latched logic output value 20 were in a logic "1" state when the pulse signal 18 was received, the latched logic value 20 would not toggle. By sensing the edge of the input

logic signal 16 and producing a pulse signal 18 therefrom, prevents the logic state of the input logic signal 16 from locking up the detection circuit (i.e., producing the chicken and egg dilemma).

Figure 2 illustrates a schematic block diagram of an edge detection circuit 25 that includes a first filter module 12, a second filter module 13, and the soft latch module 14. The first filter module 12 includes a capacitor 46, a controlled impedance 34, and an inverter 32. The controlled impedance 34 is shown to include a current source 40, p-channel transistor 36 and p-channel transistor 38. The inverter 32 is shown to include a p-channel transistor 42 and an n-channel transistor 44. The soft latch module 14 is shown to include a NAND gate 50, an inverter 52, a resistor 54, and a drive transistor 30. The drive transistor 30 is shown to include an n-channel transistor 48. The filter module 13 may include similar components to that of filter module 12 and is coupled to receive a second input logic signal 17.

The filter module 12 is operably coupled to receive the input logic signal 16 via capacitor 46. In this illustration, the filter module 12 is operably coupled to detect a falling edge of the input logic signal 16. However, as one of average skill in the art will appreciate, the filter module 12 could easily be modified to sense a rising edge of the input logic signal by using n-channel transistors in the controlled impedance 34. In the illustration shown, when a falling edge of the input logic signal 16 occurs, the drain of transistor 38 is pulled low through capacitor 46, which turns on transistor 38. Current source 40 and transistor 36 control the current flow through transistor 38 such that its impedance is of a calculated value. As is known, using the physics of semiconductor design, one of average skill in the art can readily determine the impedance of transistor 38. Note that the impedance of transistor 38 is selected with respect to the capacitance value of capacitor 46 such that the resistor-capacitor (RC) circuit formed via transistor 38 and capacitor 46 is tuned to the fall time of the edge of the input logic signal 16. This is done to prevent false triggering and to allow the input logic signal 16 to be used as a multi-input port. For example, input logic signal 16 may be coupled to a pressure sensitive switch that produces a variety of signals depending the pressure applied to the switch and the duration of the pressure.

As the source of transistor 38 is temporarily pulled low via capacitor 46, the gate of transistor 42 is also pulled low, thus turning on transistor 42. As transistor 42 turns on, transistor 44 also turns on. The drain of transistor 44 produces the pulse signal 18. Note that the time constant of the RC circuit formed by capacitor 46 and transistor 38 primarily dictates how long transistor 42 will be on, which dictates the duration of the pulse signal 18.

The soft latch logic 14 receives the pulse signal 18 via the drive transistor 30. Assume that the input signal 56 is high and, prior to the current pulse signal 18, the output of NAND gate 50 is low. Thus the input of inverter 52 is low and the output of inverter 52 is high. As the drive transistor 30 pulls the node coupling resistor 54 to NAND gate 50 low, the output of NAND gate 50 goes high. With the output of NAND gate 50 high, the output of inverter 52 goes low. When the pulse signal 18 dies out, transistor 48 turns off, but the node coupling resistor 54 to NAND gate 50 remains low latching the output of NAND gate 50 to a logic "1". In this configuration, resistor 54 provides the soft latch between the NAND gate 50 and the inverter 52. Note that resistor 54 may be intrinsic resistance built into the inverter 52. For instance, inverter 52 may be built from weak transistors with small width/height ratio.

When the latched logic value 20 (i.e., the output of NAND gate 50) is a logic "1", it will transition low when the input signal 56 is set to a logic "1" and the node coupling resistor 54 to the NAND gate 50 is temporarily pulled high. The temporary pulling of the node high may be done utilizing a second signal coupled to a capacitor that is in turn coupled to a controlled impedance, similar to controlled impedance 34. The node coupling the capacitor to the controlled impedance may be directly coupled to the node coupling resistor 54 to NAND gate 50 or indirectly coupled through a p-channel drive transistor, analogous to drive transistor 30. With either coupling, when the second signal transitions low, the controlled impedance will temporarily pull up on the node coupling resistor 54 to NAND gate 50. If this occurs when the input signal 56 is high, the latched logic value 20 will transition to a logic "0" state.

Figure 3 illustrates an edge detection circuit 60 that includes an input gate device 62, a processing module 66, memory 68, a filter module 12, and a soft latch module 14. The edge detection circuit 60 may also include a second input gate device 64, which may sense one or more

user operated switches 72 and 74. The processing module 66 may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, microcomputer, digital signal processor, central processing unit, state machine, logic circuitry, and/or any device that manipulates signals (analog or digital) based on operational instructions. The memory 68 may be a single memory device or a plurality of memory devices. Such a memory device may be a read only memory, random access memory, non-volatile memory, flash memory, system memory, magnetic tape memory, disk memory, and/or any device that stores digital information. Note that when the processing module implements one or more of its functions via a state machine or logic circuitry, the memory storing the corresponding operational instructions is embedded in the circuitry comprising the state machine or logic circuitry.

In operation, the input gate device 62 senses the state of the user operated switch 70. The user operated switch 70 may be any type of switch useable for hand-held MP3 players/recorders, CD players, digital cameras, etc. Such a switch may be, but is not limited to, a membrane switch, a toggle switch, a one-shot switch, a pressure sensitive switch, or a combination of switches. The input gating device 62 may sense the state of the user operated switch 70 via a general purpose input/output (GPIO) protocol and provides the sensed stated of switch 70 to the processing module 66 as an input logic signal 16. The processing module 66 interprets the input logic signal 16 to produce a processed logic signal 76. Depending on the type of switch 70, the processed logic signal 76 may represent one of many different commands. For example, if switch 70 is a toggle switch used to enable/disable the corresponding device, the processed logic signal 76 would be reflective of enabling/disabling the device. If, as an alternate example, switch 70 is a pressure sensitive switch, the processed logic signal 76 may be representative of volume control, enabling/disabling the device, standby mode, reset mode, set mode, etc. The filter module 12 receives the processed logic signal 76 and processes it as previously described with reference to figures 1 and 2. The soft latch module 14 receives the pulse signal 18 and processes it as previously described with reference to figures 1 and 2 to produce the logic latch value 20.

If the edge detection circuit 60 includes a second input gate device 64, multiple input logic signals may be received by the processing module 66. Based on the operational instructions, the

processing module would process each of the input logic signals to produce the processed logic signal 76. For example, one input logic signal may be representative of enabling/disabling of the device, another input logic signal may be representative of set/reset of the device, another input logic signal may be representative of mute/unmute of an output analog signal, another input logic signal may be record/play, etc. As one of average skill in the art will appreciate, multiple filter modules and associated soft latch modules may be coupled to the processing module 66 to provide the corresponding logic latch value when multiple input logic signals are being processed.

The preceding discussion presented multiple embodiments of an edge detection circuit that may be used in a highly integrated system, such as an MP3 player. By incorporating such an edge detection circuit, a highly integrated system may be set/reset, enabled/disabled, etc. without lock-ups due to fixed logic states representative of the corresponding operation. As one of average skill in the art will appreciate, other embodiments of the present invention may be derived from the teachings presented herein without deviating from the scope of the claims or the spirit of the invention.

CLAIMS

What is claimed is:

1. An edge sensitive detection circuit comprising:

a filter module operably coupled to receive an input logic signal, wherein the filter module produces a pulse signal in response to an edge of the input logic signal; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

2. The edge sensitive detection circuit of claim 1, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having a moderate impedance output, wherein an input of the first inverting logic element is coupled to the moderate impedance output, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the moderate impedance output.

3. The edge sensitive detection circuit of claim 2, wherein the first inverting logic element comprises an inverter and wherein the second inverting logic element comprises at least one of an inverter and a NAND gate.

4. The edge sensitive detection circuit of claim 1, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the capacitor and an impedance of at least one element of the gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

5. The edge sensitive detection circuit of claim 4, wherein the gating circuit comprises:

an inverter, wherein an output of the inverter is operably coupled to a drive transistor; and

a controlled impedance coupled to the capacitor, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

6. The edge sensitive detection circuit of claim 1, wherein the input logic signal is at least one of: a reset signal, a power down signal, a power up signal, a standby signal, and a set signal.

7. The edge sensitive detection circuit of claim 1 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the soft latch module latches the logic value in accordance with the second pulse signal.

8. The edge sensitive detection circuit of claim 7, wherein the second filter module comprises:

a second capacitor operably coupled to receive the second input logic signal; and

a second gating circuit operably coupled to the second capacitor, wherein the gating circuit generates the second pulse signal, wherein the second capacitor and an impedance of at least one element of the second gating circuit are tuned based on at least one of rise time or fall time of the second input logic signal.

9. A edge sensitive detection circuit comprises:

an input gating device;

a processing module operably coupled to the input gating device, wherein the processing module utilizing operational instructions to process an input logic signal from the input gating device to produce a processed logic signal;

a filter module operably coupled to receive the processed logic signal, wherein the filter module produces a pulse signal in response to an edge of the processed logic signal; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

10. The edge sensitive detection circuit of claim 9 further comprises a second gating device that provides a second input logic signal to the processing module, and wherein the filter module produces a second pulse signal in response to an edge of the processed logic signal.

11. The edge sensitive detection circuit of claim 9, wherein the input gating device provides one of a plurality of input logic signals as the input logic signal.

12. The edge sensitive detection circuit of claim 9, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having a moderate impedance output, wherein an input of the first inverting logic element is coupled to the moderate impedance output, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the moderate impedance output.

13. The edge sensitive detection circuit of claim 9, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the capacitor and an impedance of at least one element of the gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

14. The edge sensitive detection circuit of claim 13, wherein the gating circuit comprises

an inverter, wherein an output of the inverter is operably coupled to a drive transistor; and

a controlled impedance coupled to the capacitor, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

15. The edge sensitive detection circuit of claim 9, wherein the input logic signal comprises at least one of: a reset signal, a set signal, a power down signal, a power on signal, and a standby signal.

16. The edge sensitive detection circuit of claim 9 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the soft latch module latches the logic value in accordance with the second pulse signal.

17. An edge sensitive detection circuit comprising:

a capacitor operably coupled to receive the input logic signal;

a controlled impedance coupled to the capacitor, wherein the capacitor and an impedance of at least one element of a gating circuit are tuned based on at least one of rise time or fall time of the input logic signal;

an inverter, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor;

a drive transistor operably coupled to produce a pulse signal, wherein an output of the inverter is operably coupled to the drive transistor;

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

18. The edge sensitive detection circuit of claim 17, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having a moderate impedance output, wherein an input of the first inverting logic element is coupled to the moderate impedance output, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the moderate impedance output.

EDGE SENSITIVE DETECTION CIRCUIT

ABSTRACT OF THE DISCLOSURE

An edge sensitive detection circuit includes a filter module and a soft latch module. The filter module is operably coupled to receive an input logic signal that corresponds to the triggering of an event and produces a pulse signal in response to an edge of the input logic signal. The filter may include a capacitor operably coupled to a controlled impedance, an inverter and a driver transistor, wherein the capacitor senses an edge of the input logic signal and, in combination with the controlled impedance, produces the pulse signal. The soft latch module is operably coupled to receive the pulse signal and to latch a logic value in accordance with the pulse signal.

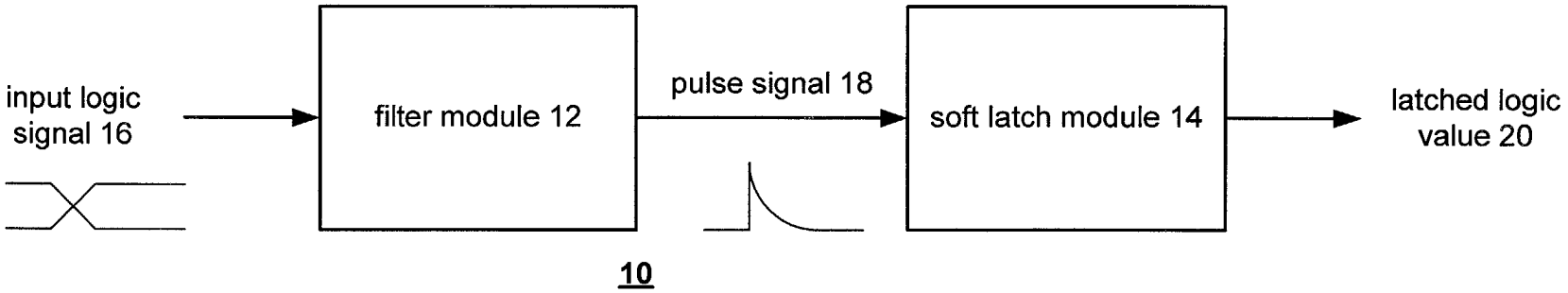
input logic signal 16
filter module 12
pulse signal 18
soft latch module 14
latched logic value 20
10

FIG. 1

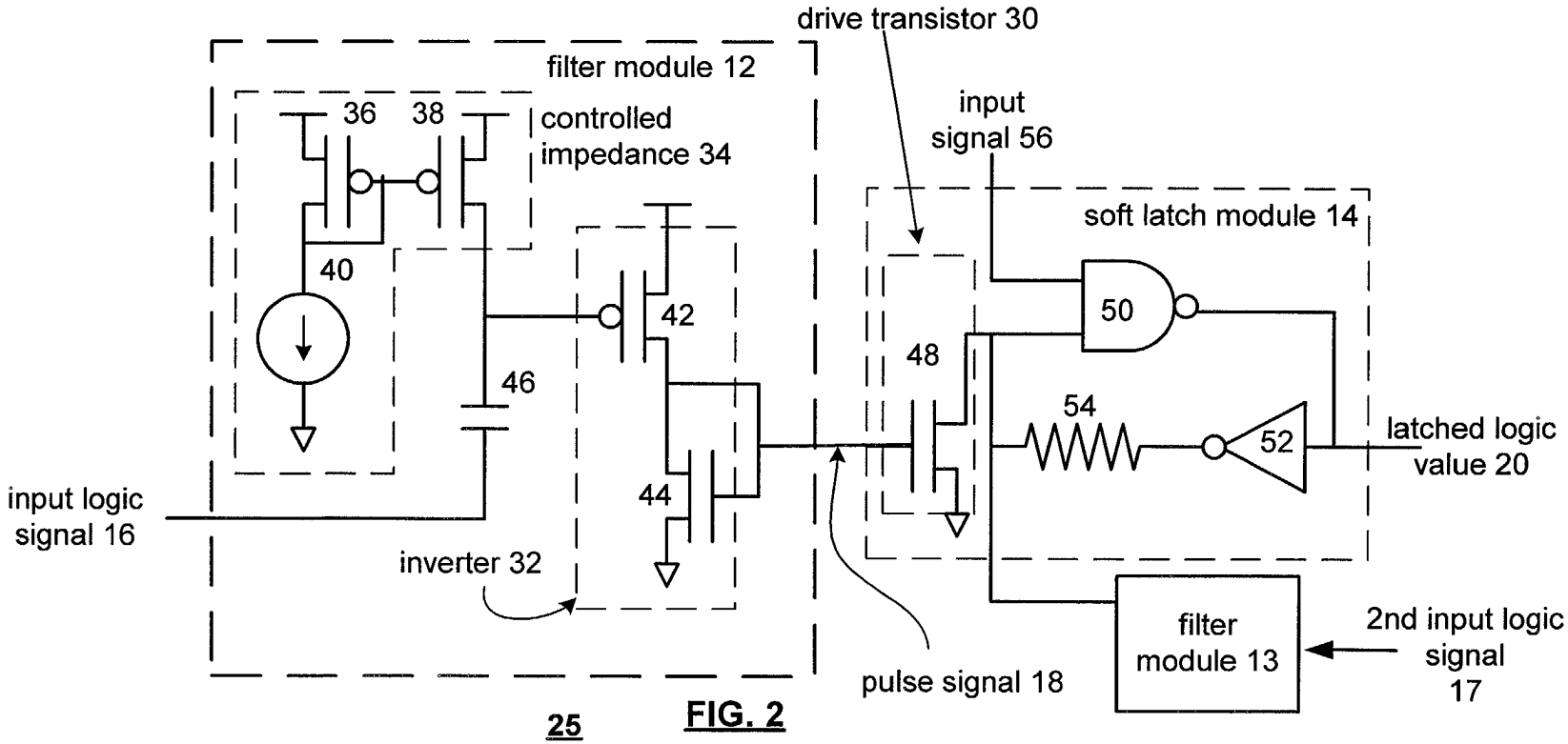
drive transistor 30
filter module 12
input signal 56
36
38
controlled impedance 34
soft latch module 14
40
42
50
48
46
54
52
latched logic value 20
input logic signal 16
44
inverter 32
filter module 13
2nd input logic signal 17
pulse signal 18
25

FIG. 2

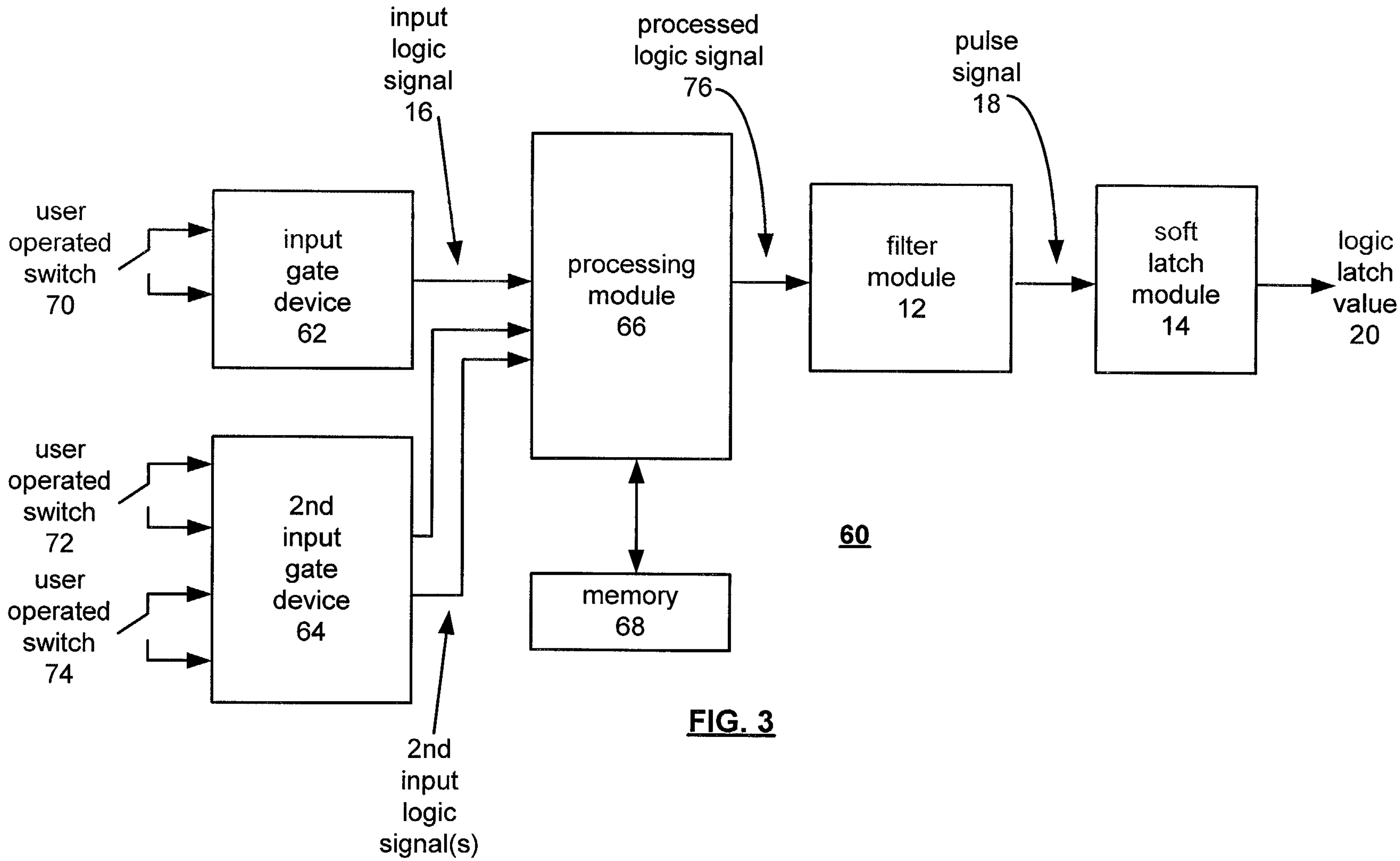
input
logic
signal
16
processed
logic signal
76
pulse
signal
18
user
operated
switch
70
input
gate
device
62
processing
module
66
filter
module
12
soft
latch
module
14
logic
latch
value
20
user
operated
switch
72
user
operated
switch
74
2nd
input
gate
device
64
memory
68
60
2nd
input
logic
signal(s)

FIG. 3

PATENT APPLICATION
Docket No.: SIG000049

DECLARATION AND POWER OF ATTORNEY
Pursuant to 37 C.F.R 1.63 and 1.67

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name; and
I believe that I an inventor of the subject matter of a patent application entitled:

EDGE SENSITIVE DETECTION CIRCUIT

The specification for the patent application (check one):

[X] is attached hereto.

[ ] was filed on as Application Serial No.
and was amended on (if applicable).

[ ] was filed as PCT International Application No. PCT/ on
and was amended on (if applicable).

[ ] was filed on as Application Serial No.
and was issued a Notice of Allowance on

I hereby state that I have reviewed and understood the contents of the above identified patent application, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this patent application as defined in 37 C.F.R. Section 1.56. If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 C.F.R. Section 1.56 which became available between the filing data of the prior application and the national or PCT international filing date of this CIP application.

I hereby claim foreign priority benefits under 35 U.S.C. Sections 119 and 365 of any foreign application(s) for patent(s) or inventor's certificate(s) listed below. I have also identified below any foreign application(s) for patent(s) or inventor's certificate(s) filed by me or my assignee which: disclose the subject matter claimed in this patent application; and have a filing date that is either: (1) before the filing date of the application on which my priority is claimed; or, (2) before the filing date of this application when no priority is claimed:

Prior Foreign Patents
(list number, country, filing date MDY, date laid open, date granted or patented)

I hereby claim the benefit under 35 U.S.C. Sections 120 and 365 of any United States application(s) listed below and PCT international application(s) listed below:

Prior U.S. or PCT Applications

Application No.	Mo/Day/Yr Filed	Status

I hereby appoint Timothy W. Markison, Registration No. 33,534 of SigmaTel Inc., 2700 Via Fortuna, Sutie 500, Austin, Texas 78746 as my attorney, with full power of substitution and revocation, to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith, and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty, and I hereby authorize him to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary.

Please address all correspondence and direct all telephone calls to:
SigmaTel, Inc.,
2700 Via Fortuna
Suite 500
Austin, Texas 78746
Phone: (512) 381-3732
Fax: (512) 381-4125
Customer No: 000024263

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this patent application or any patent issued thereon.

Inventor(s)

May Michael R. 1213 Shannon Oaks Trail Austin Texas 78746	citizen of: US	Signature: Michael R. May Date: 7/27/00
	citizen of:	Signature: _____ Date: _____
	citizen of:	Signature: _____ Date: _____
	citizen of:	Signature: _____ Date: _____
	citizen of:	Signature: _____ Date: _____
	citizen of:	Signature: _____ Date: _____